Reg. No. : | | | | | | | | | | | | |

Question Paper Code : 30517

B.E./B.Tech. DEGREE EXAMINATIONS, NOVEMBER/DECEMBER 2024.

Sixth/Seventh Semester

Electronics and Communication Engineering

EC 8095 — VLSI DESIGN

(Common to Electrical and Electronics Engineering/Electronics and Instrumentation Engineering/Electronics and Telecommunication Engineering/Instrumentation and Control Engineering/Robotics and Automation)

(Regulations 2017)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Draw a 4:1 multiplexer using transmission gate.

2. Draw the DC transfer characteristics of CMOS inverter.

3. State the different types of power dissipation in CMOS circuits.

4. Draw a 2-input XNOR using NMOS pass transistor.

5. State the cause of monostability problem in sequential circuits.

6. Differentiate latch and flip-flop.

7. State the use of Barrel shifter.

8. Differentiate SRAM and DRAM.

9. State the merits of BIST.

10. Mention the need for DFT.

PART B — (5 × 13 = 65 marks)

11. (a) (i) Derive an expression for the rise time and fall time delay in a CMOS inverter. (8)

(ii) Draw the stick diagram of a 2-input CMOS NAND gate. (5)

Or

(b) (i) Derive the necessary condition if both PMOS and NMOS in CMOS inverter operates in saturation region. (5)

(ii) Give short notes on scaling in MOSFET. (8)

12. (a) (i) Derive an expression for the dynamic power dissipation in CMOS circuits. (8)

(ii) Design a 3-input NAND gate using dynamic CMOS logic. (5)

Or

(b) Design a half adder using static CMOS logic and transmission gate. Analyze the hardware complexity.

13. (a) Design a D-latch using NMOS pass transistor. Using which design a positive edge triggered D-flipflop using NMOS pass transistor.

Or

(b) Elucidate in detail with neat diagram astability in sequential circuits.

14. (a) Design a 8-bit signed multiplier using radix-4 booth encoding. Explain with an example.

Or

(b) With neat diagram, explain the design of a 4-bit barrel shifter and mention its applications.

15. (a) Give short notes on FPGA interconnect routing architecture with neat diagram.

Or

(b) (i) With neat block diagram, enumerate in detail BIST architecture. (8)

(ii) Explain Linear Feedback Shift register which can be used to generate the test patterns with an example. (5)

PART C — (1 × 15 = 15 marks)

16. (a) Derive the necessary sum and carry out expressions of a 4-bit carry look ahead adder. Design a 4-bit adder using dynamic CMOS logic and static CMOS logic. Analyze the hardware complexity.

Or

(b) (i) Design a 4-transistor DRAM memory cell and explain read and write operation. (7)

(ii) Design a 3-bit even parity generator only using NAND gates and realize using static CMOS logic. (8)